Investor Relations NEXTIN, Inc.

Next Inspection Solutions for Semiconductor Applications

November 18th, **2024**

Chris Park / CEO





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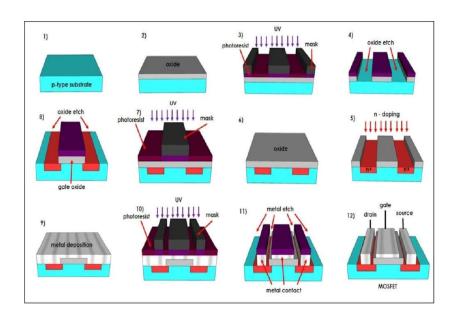


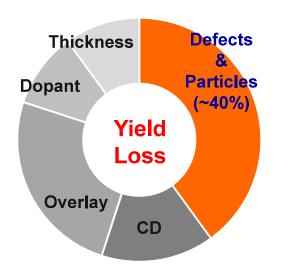
Market Analysis

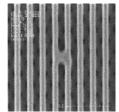


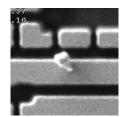
Wafer Inspection Process

- Fabrication of semiconductor devices has 3,000+ unit process such as lithography, etch, film deposition, ion implantation,
- Wafer inspection process is detecting pattern defects and particles which cause yield loss of device fabrication processes





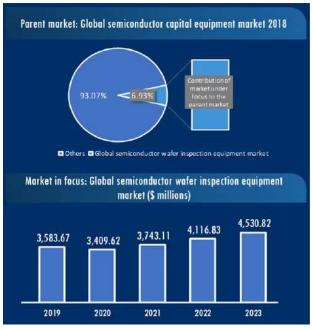




Wafer Inspection Process(2)

- Fabrication of advanced devices requires inspection process more and more
- Metrology & Inspection tool market size: 10% of Fab CAPEX @ Samsung
- Optical Inspection Tool Market Size: 5.5% of Fab CAPEX(Technavio Report 2019)

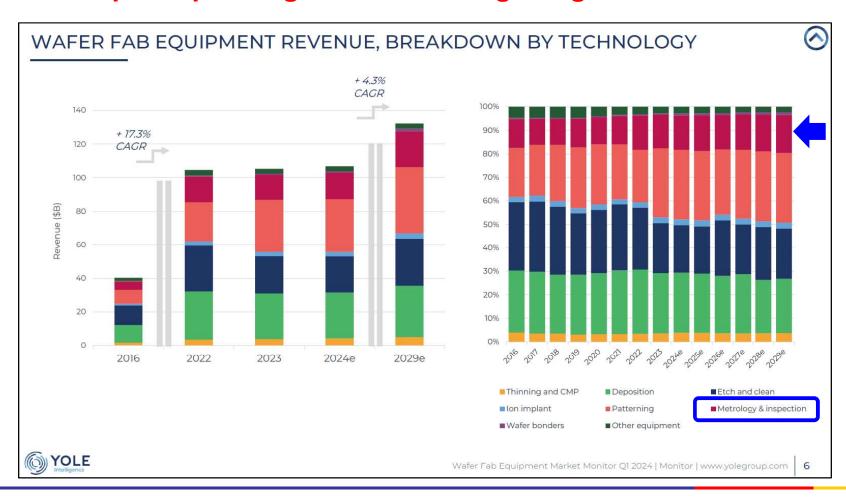






Importance of Wafer Inspection

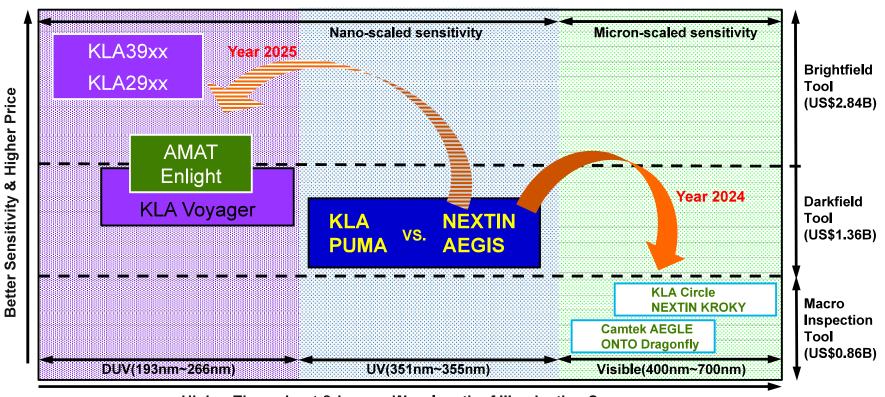
The capital spending for MI tools is getting more and more!!!





Optical P-Wafer Inspection Tools

- Wafer fabs execute mix-and-match strategy between tools and suppliers
 - BF, DF and Macro tools have its own advantages and applications
 - Suppliers have its own technology and strengths in defect detection







NEXTIN Products



AEGIS Evolution (DF Tool)

Cost-effective solution over the competitor !!!





2020









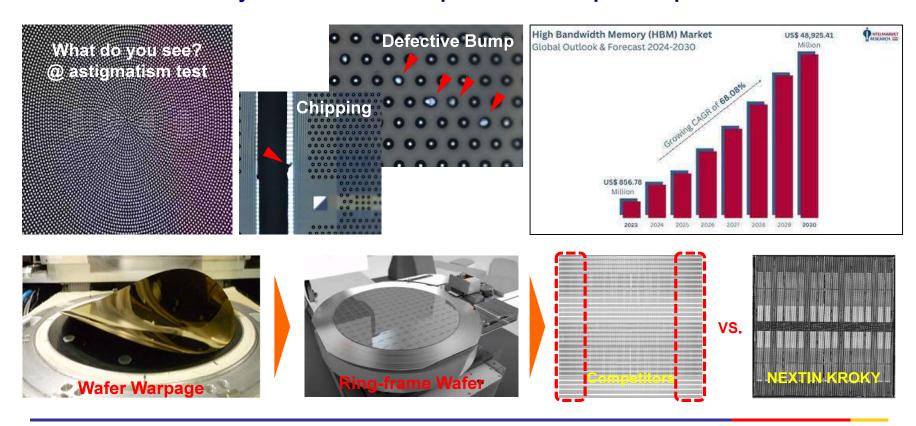
AEGIS-XT (Higher X-put) 2016



AEGIS-DP

KROKY for HBM (Macro Tool)

- Advanced HBM gets bigger warpage than depth-of-focus (optical detection limit)
- KROKY resolves the difficulty with patented optic technology and algorithm
- KROKY is the only solution over competitors at competitive price !!!



IRIS for 3D Process

- Moore's Law keeps going on lateral scaling with vertical stacking 3D Memory
- It requires paradigm shift in inspection technology surface to buried defects
- Intel and NEXTIN presented new 3-dim. inspection technology at SPIE 2021
- IRIS is the only solution for very highly stacking processes !!!

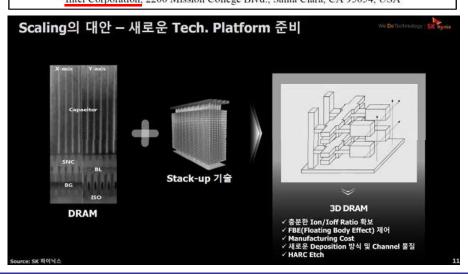
Comparative near infrared through-focus scanning optical microscopy for 3D memory subsurface defect detection and classification

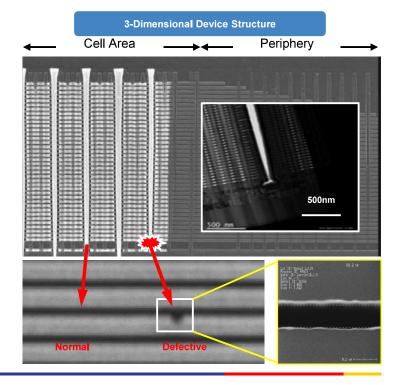
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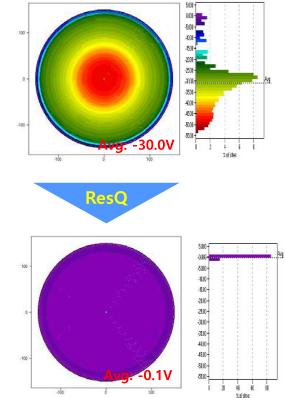




ResQ for EUV Process

- Even weak electrostatic charges cause yield killing defects at <10nm design node</p>
- Buried electrostatic charges should be removed before critical processes
- ResQ newly adds up electrostatic charge removal process at advanced process !!!







Business Strategy



Business Strategy

- Keep releasing next generation models on time: AEGIS-IV in 2025
- Secure the existing customers with localization in China
 - 无锡纳科鑫科技有限公司:
 - Production start: KROKY(Q3 2025) & AEGIS (Q1 2026)
- Engage with new customers: HHG, Intel, Micron, Kioxia, SONY, Infineon, GF, ...

- Make more success stories & value @ top-tier customer: KROKY, IRIS & ResQ
- Fan out with the success stories to other customers
- Keep developing next generation models to maintain performance gaps

Thanks you !!!

